ULTRA-LIGHT AMORPHOUS SILICON CELL FOR SPACE APPLICATIONS

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ABSTRACTS

For space applications, solar cells should be optimized for highest power density rather than for highest efficiency. In this context, relatively low efficiency thin-film solar cell may well surpass multi-junction III-V based solar cells if they can be made thin enough. In thin-film solar cells the power density is mostly limited by the substrate. The introduction of ultra-thin polymeric substrates is the key for decreasing the cell mass. In this work, a very thin polyimide film LaRC™-CP1 was used as substrate or superstrate for amorphous silicon solar cell fabrication. CP1 films were either fixed on a glass carrier or spin coated onto a glass carrier coated with a release agent. By depositing amorphous silicon cells on 6 µm thick CP1 films, a power density of 2.9 W/g under AM1.5g and of 3.9 W/g (estimated) under AM0 illumination spectra was achieved, in substrate (n-i-p) configuration (for a cell area of ca. 0.25 cm^2). A similar cell deposited in superstrate (p-i-n) configuration exhibits a record power density of 3.2 W/g under AM1.5g and an estimated value of 4.3 W/g under AM0 illumination spectra. Release of the finished solar cells from the glass carrier was also tested.

INTRODUCTION

For space applications, solar cells should be optimized for highest power density rather than for highest efficiency. The best power density has so far been obtained with multi-junction III-V based solar cells; a power density value of 3 W/cm^2 was recently demonstrated using a InGaP/GaAs cell configuration [1]. Current commercial best products based on Ge/III-V multi-junction (improved triple-junction) solar cells have a mass of 840 g/m² and a power density of 370 W/m² for an AM0 efficiency of 27% (for nude unwired cells).

Alternatively, thin-film solar cells deposited on very thin substrates offer promising possibilities. Even though efficiency values are much lower, the reduction in substrate thickness can compensate for the loss. For example CIGS cells with an efficiency of 14.2% (under AM1.5) have been deposited on 25 µm thick Ti foils for space applications [2]. On the same substrate, 15% AM0 efficiency have been obtained for 27 cm^2 CIGS cells, which corresponds to a power density of ca. 1 W/g [3]. Power densities over 1.2 W/g have recently been demonstrated by the deposition of a-Si:H based triple junction cell onto 25 µm thick polyimide films [4].

a-Si:H (hydrogenated amorphous silicon) is a proven radiation hard material. In case of proton irradiation, it tolerates fluences 10 times larger than GaAs or more than 100 times larger than c-Si for the same relative degradation of solar cells (at any given proton energy). The hardness of a-Si:H cells are here at least equivalent to that of cells based on CIGS or CdTe [5, 6]. Furthermore, defects created by proton irradiation can be easily annealed out, even at temperatures around 100°C [7]. Due to the relatively high operation temperature of the cell in space, very limited degradation of a-Si:H solar cell is therefore expected in space.

Even though best a-Si:H cells efficiency is obtained on glass substrates [8], other type of substrates such as metal or polymers foils can be used without much loss in efficiency [9, 10]. As in thin-film solar cells the power density is mostly limited by the substrate, the introduction of ultra-thin polymeric substrates is the key for decreasing the cell mass. For this purpose, a-Si:H single-junction cells were deposited on a 6 µm fluorinated polyimide LaRC™-CP1 developed originally for space applications by NASA and licensed to SRS Technologies. CP1 exhibits a high UV resistance and is compatible with space environment; this material is already qualified for space flights. CP1 can be easily cast or spin-coated resulting in uniform and flat films and has a glass transition temperature of 263°C. CP1 is therefore well suited for solar cell applications. The material is highly transparent and UV resistant and both substrates and superstrates cell configuration can be considered.

Fabrication of ultra-thin sheets of CP1 is already well mastered (from small to very large sizes) and the fabrication and test deployment of a 400 m^2 solar sail using CP1 has been achieved [11]. 400 m² of CP1/a-Si:H cells would generate a power of ≥40 kW. Beside the compatibility of the solar process with the film materials, deposition of solar cells on ultra-thin sheets is a critical issue. In order to facilitate the handling of ultra-thin foils, CP1 was spin coated on *a temporary* glass carrier. With this approach, all cell processes can be performed on a rigid substrate using standard thin-film silicon deposition equipment. As a last step, the CP1 film with the solar cell is released from the glass substrate. This fabrication strategy is therefore fully compatible with industrial a-Si:H based solar cell production facilities (such as UNAXIS KAI reactors [12]), and would allow a rapid market entry of ultra-thin a-Si:H modules, in large quantity and sizes. Production of ultra-lightweight, high powered space solar arrays in the +50 kW range could hence be envisage in close future.

EXPERIMENTAL

Several cells were deposited on CP1, either in substrate (n-i-p) or superstrate (p-i-n) configurations by VHF PE-CVD (Very High Frequency Plasma Enhanced Chemical Vapor Deposition) at temperatures around 200°C [[13]. Several cells in superstrate (p-i-n) configurations were also deposited in a KAI S reactor at 40 MHz [14]. All depositions were performed on substrates (or superstrates) with sizes ranging between 4x4 cm^2 and 8x8 cm^2.

In n-i-p configuration, CP1 films (ca. 6 µm thick) were fixed with polyimide tape on a glass substrate and then coated with a rough Cr/Ag/ZnO:Al back reflector by sputtering. After the deposition of the a-Si:H n-i-p cell, a top ZnO:B laser was deposited by low pressure CVD (LP-CVD) and patterned to defined diodes with an area of ca. 0.25 cm^2. Finally the a-Si:H cell was also patterned using the ZnO top contact as a mask.

In p-i-n configuration, a CP1 film was first spin-coated on a glass substrate (glass carrier) coated with a release agent. A ZnO:B top contact was then deposited by LP-CVD, followed by the deposition of a p-i-n cell, and of a ZnO:B bottom contact. Finally, the bottom ZnO contact and the cell were also patterned using the same process used for the n-i-p configuration. Several releasing formulations were also applied on the glass carrier and tested. In order to secure the CP1 film on the carrier and ease the cell release, polyimide tape was applied on the edge of the CP1/glass carrier. Release was then achieved by pulling the tape.

Measurements of the external quantum efficiency (EQE) were performed under white light bias illumination to deduce total cell current under AM1.5g and AM0 illumination. Measurements of the I(V) characteristics were performed on a two light sources WACOM solar simulator under a AM1.5g spectrum at 100 mW/cm^2. Power outputs of the cells under AM0 were simply estimated assuming the same efficiency for AM0 as for AM1.5 irradiations. This approach was cross-checked by estimating the current under AM0 from EQE measurements, and assuming standard variation of V_{oc} and FF with the current. The power densities were calculated from the various thickness of the layer stack, assuming nominal densities. For the cells deposited in the p-i-n configuration, cell performances were measured with the CP1 (and the cell) attached to the glass carrier. No corrections were made for the optical loss induced by the glass carrier.

RESULTS AND DISCUSSION

The respective performances of small area cells fabricated in both substrate and superstrate configurations are presented below and summarized in Table 1 (best cell results).

Substrate cell configuration

A picture of a piece of CP1 with several n-i-p a-Si:H solar cells is shown in Fig. 1. The I(V) characteristics under AM1.5 as well as the EQE for the best cell are plotted in Fig. 2. These data are obtained for cells with an intrinsic layer thickness of 350 nm in the initial (non degraded state) with a 2.1 µm thick top ZnO layer.

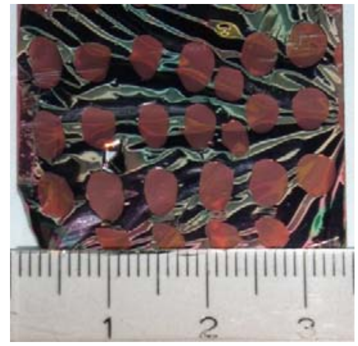

Fig. 1: Picture of n-i-p single-junction a-Si:H cells deposited on CP1 coated with a rough ZnO/Ag back reflector. Diodes are defined by the patterning (by hand) of the ZnO layer followed by an etching of the a-Si:H layers.

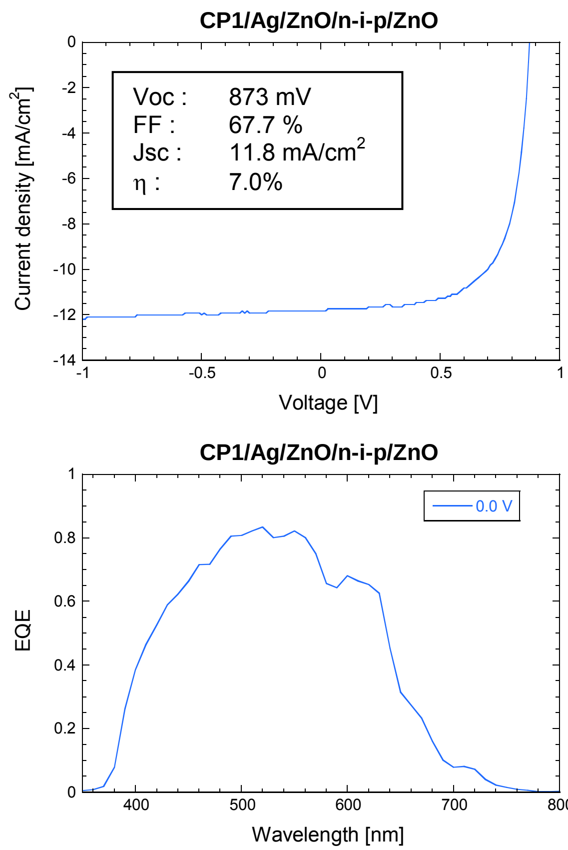

Fig. 2: I(V) characteristics under AM1.5g illumination (left) and external quantum efficiency at 0 V (right) of a n-i-p single-junction a-Si:H cell deposited on CP1 coated with a ZnO/Ag back reflector, as shown in Fig. 1.

The efficiency obtained here is a bit lower than state-of-the-art efficiency achieved using thick polyimide or glass substrates [9]. As seen in the EQE curve (Fig. 2), the response in the blue shows losses due probably to a too thick p-layer. Furthermore, the interference fringes as well as the relatively low response around 700 nm indicates that the back reflector roughness is not high enough (for enhanced light diffusion and optimal light-trapping) resulting in a rather low short-circuit current value. A comprehensive optimization of the cell (which has not yet been performed) should be able to correct these weaknesses.

During the processing, the piece of CP1 was several times detached from the glass carrier, rolled, unrolled and re-attached to the glass carrier. No damaging or peeling-off the cell was observed despite the small curvature radius of about a few millimeters in the rolled state. CP1/a-Si:H cells are very flexible.

Superstrate cell configuration

Several cells with an intrinsic layer thickness of 300 nm were deposited on CP1 spin-coated on glass carrier with 1.8 µm thick top and bottom ZnO contacts. No additional back reflector was implemented. Performances of the cells were determined on the cell attached to the glass carriers, without any correction for the transmission through the glass. The I(V) characteristics under AM1.5g as well as the EQE for the best cell are plotted in Fig. 3.

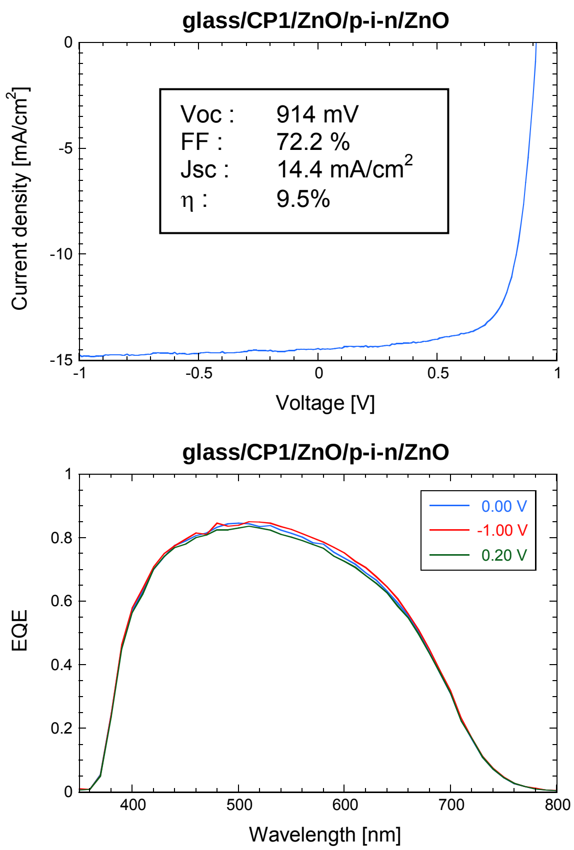

Fig. 3: I(V) characteristics under AM1.5g illumination (left) and external quantum efficiency at various bias voltage values (right) of a p-i-n single-junction a-Si:H cell deposited on CP1 coated with a ZnO front contact. A back ZnO was used as back contact /back reflector.

Compared to the results in the n-i-p configurations, both I(V) and EQE results are improved. Thanks to the very efficient light-trapping created by the texture of the LP-CVD deposited ZnO [15], both a high short-circuit current and high response in the red and infra red region of the EQE are obtained. Higher efficiency could possibly be obtained by incorporating also a white reflector at the back. However, this may result in a larger weight and lower power density. Implementation of a thin ZnO/Ag could be the optimal solution (in term of power density).

Several formulations were tested for the release of the CP1 film and the cells from the glass carrier. The best formulation allows the release of the sample simply by pulling the polyimide tape used to secure the CPI film during processing (see Fig. 4). No additional treatment is required after the cell fabrication and the release process is not affected by the previous processing steps.

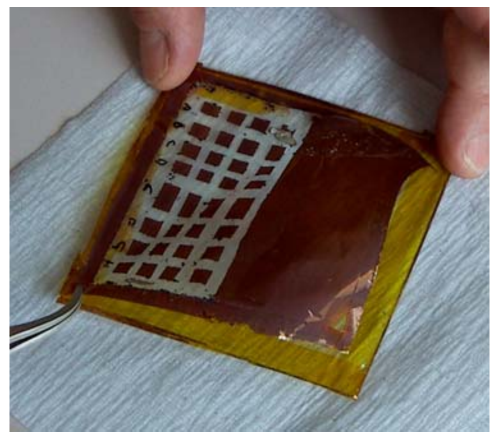

Fig. 4: Picture of the release of a 6 µm thick CP1 films with test cells in the p-i-n configurations from the glass carrier. Polyimide tape was used to secured the CPI film during processing and rigidify the sample after release.

So far, cells in the p-i-n configuration tend to get damaged during the release of the CP1 due to a poor adhesion of the front ZnO contact on the CP1 film causing a partial peeling off of the cells as well as shunts. A surface treatment or an interface layer should be devised to solve the problem. The ZnO layer itself (and its introduction in a cell) seems not to be an issue as no particular problem was observed in the case of the n-i-p configuration incorporating such a layer a the top transparent contact.

Cell structure	Cell thickness [µm]	Total thickness [µm]	Density (total) [mg/cm^2]	Efficiency (under AM1.5g)	Power output [mW/cm^2]		Power density [mW/g]	
					AM1.5g	AM0	AM1.5g	AM0
n-i-p	0.35	9.05	2.4	7.0	7.0	9.5	2900	3900
p-i-n	0.30	10.25	3.0	9.5	9.5	12.8	3200	4300

Table 1: Density, efficiency, power output and power density for the best cells in n-i-p and p-i-n configurations. Values are indicated for a nude, non-encapsulated cell. Details on the cell structures are given in the text.

CONCLUSIONS

Power needs for new communication satellites are rapidly increasing and, as the size and weight increase, require new innovative photovoltaic (PV) technologies. For long mission, ion thrusters are very appealing due to their very high specific impulse and high fuel efficiency but require very high amount of energy which can hardly be supplied with traditional PV arrays. The best PV arrays exhibit power density of ca. 100 W/kg using high efficiency rigid solar cells with inflatable deployment systems concentrator lens solar arrays.

High altitude airships are currently in development to replace or complement communication satellites. These airships will be operated by solar energy and flown at very high altitude above the atmospheric currents. For this application, solar arrays with a high specific energy density are required and values above 1000 W/kg are desired.

Despite lower efficiency (compared to crystalline solar cells based on c-Si or GaAs), thin-film solar cells can achieve very high power density if the substrate can be made thin (and light) enough. Even though a-Si:H solar cells do not perform (in term of efficiency) as well as cells from other thin-film technologies, the low process temperature and the compatibility with a variety of substrates and compliance to low cost, large scale manufacturing processing are key advantages for CP1/a-Si:H. a-Si:H cells can be deposited on ultra-thin CP1 polymeric substrate leading to record power densities.

LaRC™-CP1 is a fluorinated polyimide film originally developed by NASA which is qualified for space flights and already used in the satellite industry. Its properties together with the fact that it can be spin-cast or spin-coated to form ultra-thin (a few micrometers thick) sheets are very attractive for a use as substrates for PV arrays.

Single-junction a-Si:H cells were deposited on CP1 in n-i-p or p-i-n configurations. Initial efficiencies of 9.5% have been achieved under AM1.5g with a record power density of 3.2 W/g and an estimated value of 4.3 W/g under AM0. These cells were fabricated using standard process, as used for deposition on glass, on glass carrier spin-coated with CP1. In the p-i-n configuration some peeling off of the ZnO layer was observed which will require optimization or modification of the CP1/ZnO interface. An optimal cell design has yet to be devised to permit a trouble free release from the carrier (without peeling off) while maximizing power density. In contrast no peeling off of the cell was observed in the in the n-i-p configuration despite several rolling/unrolling of the CP1 substrate. Full compatibility of LaRC™-CP1 for n-i-p configuration is therefore demonstrated, while p-i-n may require some modification of the top transparent conductive oxide (for the time being a LP-CVD deposited ZnO layer is used).

Regarding the cell deposition, all processing steps are fully compatible with industrial production equipment such as KAI reactors developed by UNAXIS; an up-scaling of the fabrication up to sizes of 1.4 m^2 is straightforward. However, for module fabrication one additional issue has to be addressed, namely the integration of a monolithic serial connection. Industrial solutions exist for thicker polymeric substrates which could be adapted for ultra-thin CP1 substrates. Additional coatings for module protection or cooling could also be needed depending on the application.

Having solved the problem of monolithic serial connection, bus wiring on the PV array can be kept to a minimum, greatly reducing the weight of the interconnects as compared to present technologies. Furthermore, due to the very light weight of the modules, no reinforcement, protective coverslides, or other mass add-ons should be required to withstand the high G-forces of space launch. Finally, deployment schemes already developed for 20 meter solar sails should allow for a straightforward design and fabrication of space arrays with power ≥50 kW or to consider multiple arrays deployments for higher power values.

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